information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

34. (Once Amended) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device [having a first operation] operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the [first operation] burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

35. (Once Amended) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst [access] extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank.

37. (Once Amended) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of [a first type of] burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the [first type of] burst extended data out memory and a second set of requirements for the second type of memory.

38. (New) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of

access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively.

39. (New) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank.